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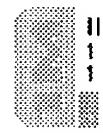
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Rawski, M.; Jozwiak, L.; Nowicka, M.; Luba, T.;
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1 Structural gate decomposition for depth-optimal technology mapping LUT-based FPGA design

Cong, J.; Yean-Yow Hwang;

Design Automation Conference Proceedings 1996, 33rd , 3-7 June 1996

Pages:726 - 729

[Abstract] [\[PDF Full-Text \(388 KB\)\]](#) IEEE CNF

2 On area/depth trade-off in LUT-based FPGA technology mapping

Cong, J.; Yuzheng Ding;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 2 , Issue: 2 , June 1994

Pages:137 - 148

[Abstract] [\[PDF Full-Text \(1072 KB\)\]](#) IEEE JNL

3 DAOmap: a depth-optimal area optimization mapping algorithm for designs

Chen, D.; Cong, J.;

Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM International Conference , 7-11 Nov. 2004

Pages:752 - 759

[Abstract] [\[PDF Full-Text \(908 KB\)\]](#) IEEE CNF

4 Hermes: LUT FPGA technology mapping algorithm for area minimization with optimum depth

Teslenko, M.; Dubrova, E.;

Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM International Conference , 7-11 Nov. 2004